ULTRA-WIDEBAND DIGITAL BEAMFORMER WITH SIGNIFICANT SWAP-C REDUCTION

Elias A. Alwan (The Ohio State University, Columbus, Ohio, USA, alwan.2@osu.edu); Sidharth Balasubramanian (The Ohio State University, Columbus, Ohio, USA, balasubramanian.35@osu.edu); Jad G. Atallah (Notre Dame University - Louaize, Lebanon, jatallah@ndu.edu.lb), Matthew Larue (The Ohio State University, Columbus, Ohio, USA, larue.68@osu.edu); Kubilay Sertel (The Ohio State University, Columbus, Ohio, USA, sertel@ece.osu.edu); Waleed Khalil (The Ohio State University, Columbus, Ohio, USA, khalil@ece.osu.edu); John L. Volakis (The Ohio State University, Columbus, Ohio, USA, volakis@ece.osu.edu)

ABSTRACT

We propose a novel transceiver architecture for cognitive sensing. The architecture supports agile beam forming, jamming mitigation, as well as MIMO communications. An essential aspect of the new architecture is its departure from the traditional digital beamforming approaches. Specifically, a single ADC is assigned to a group of array elements instead of having one ADC per element. To facilitate this approach, code division multiplexing is applied to each received antenna signal prior to combining them for digitization using a single ADC. Thus full signal recovery is possible at digital baseband via decoding. The proposed architecture significantly reduces the number of ADCs and I/O channels and hence drastically improves size, weight, area, power and cost of the system with minimal impact on receiver signal-to-noise ratios.

1. INTRODUCTION

Antennas with advanced spatial filtering have been a popular research topic in the past decade. They provide the ability to accurately steer the beam towards a designated target while improving rejection of interferers. Typically, beamforming has been used in applications such as radar systems, wireless communications, surveillance, radio astronomy, sonar, and audio fields [1]. However, so far, to enable beamforming a wideband feed network that scans down to 70^{o} from normal is required. This is a highly expensive and even impractical approach for wideband applications.

Undoubtedly, there is a strong interest to enable low-cost beamforming over large bandwidths. This will allow for a single transceiver to enable simultaneous sensing of the whole space over a wide spectrum. Concurrently, cognitive sensing over a wide bandwidth can be realized [2]. Indeed, the successful integration of wideband back-end components into a single conformal low cost, low weight and highly multifunctional structure would lead to transformational utilizations of wideband phased arrays.

Conventional RF beamformers are typically based on true-time delay (TTD) phase shifters, known to suffer from area, cost and bandwidth limitations [3]. Recently, digital beamformers have been advocated due to their waveform agility and wideband operation. However, existing digital beamformers at the baseband suffer from several issues, limiting them to small arrays (i.e. <10). In particular, they suffer from high cost level, power consumption and hardware complexity due to the large number of analog-to-digital converters (ADCs).

In this paper, we propose a reduced-hardware digital beamforming transceiver architecture suitable for large array systems. More specifically, we use on-site coding to significantly reduce the number of ADCs and hence the number of parallel input/output (I/O) channels. This approach implies a substantial reduction in the number of field-programmable gate arrays (FPGAs) needed for baseband processing.

The paper is organized as follows: section 2 provides a brief overview of existing beamforming techniques and their limitations. This is followed by the proposed beamformer architecture in section 3. Section 4 expands on the topic by considering ultra wideband (UWB) systems. Simulations for the proposed digital beamformer are given in sections 5 and 6.

2. EXISTING BEAMFORMING TECHNIQUES

Let us consider a linear equally-spaced array of M-elements with spacing d. As shown in Fig. 1, the array is illuminated by an plane wave incoming at an angle θ_1. Hence, the required time delay for each antenna element is computed as

$$\tau_{\mathrm{M}} = \frac{(M-1)\, d \sin\theta_1}{c} \qquad (1)$$

where c is the speed of light. This delay on each element steers the array in a desired direction and blocks reception

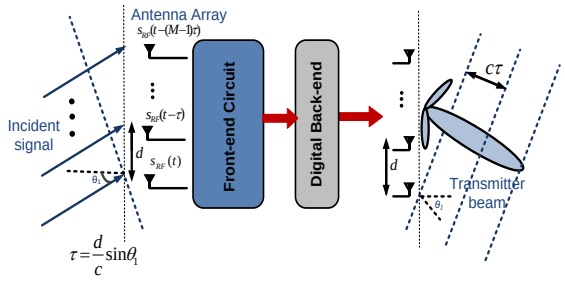

Fig. 1. Linear, equally-spaced array for beamforming.

from other directions. Beamforming can then be realized in a number of ways: (1) using phase shifters behind each antenna (a.k.a. RF beamforming), (2) adjusting the phase of the local oscillator (a.k.a. LO phase shifting), or (3) via post processing after digitization (a.k.a. digital beamforming). As can be realized, the former two schemes belong to the class of analog beamforming.

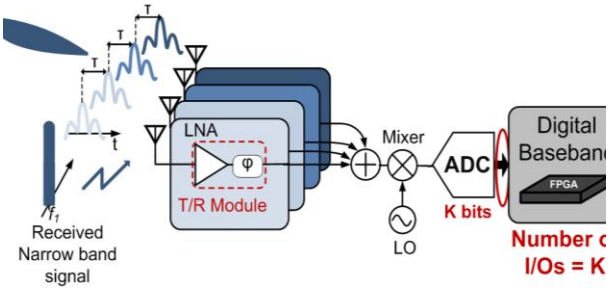

Fig. 2. Analog beamformer using phase shifters implemented along the signal path.

2.1. Analog Beamformers

As depicted in Fig. 2, the analog front-end of a receiver typically starts with a low noise amplifier (LNA). Right after the LNA, either TTD elements or phase shifters are implemented in the signal path to perform beamforming.

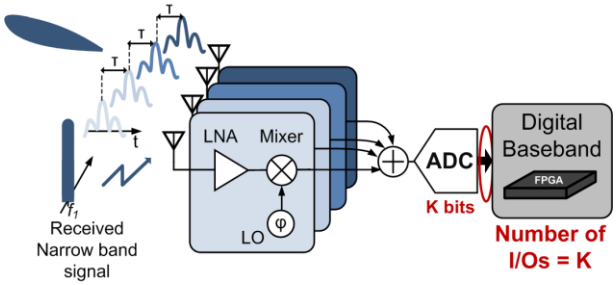

Fig. 3. Analog beamformer using phase shifters implemented at the local oscillator.

Typically, for wideband reception, phased arrays make use of TTD elements [4]. However, TDDs suffer from high losses and bandwidth limitations. This is even more compounded for arrays with a large number of elements as they require a large number of phase shifters. This leads to a drastic increase in the size, weight and complexity of the array not to mention power consumption. Further, due to their limited phase tuning, analog phase shifters can only sense a single spatial direction at a time [2]. That is, beams from multiple directions cannot be formed simultaneously, limiting the capability of the beamformer, particularly for MIMO applications. Nevertheless, a major advantage of analog beamforming at the RF front-end is the use of a single mixer to perform frequency translation. As such, the combined RF signal is down-converted to an intermediate frequency (IF) that can be digitized by a single ADC for post processing.

Taking advantages of the single mixer, beamforming complexity can be reduced by performing the phase shifting at the LO. This is illustrated in Fig. 3. In this case, no phase shifting loss incurs and receiver sensitivity is not impacted. In fact, non-linearity and loss can be tolerated in the LO path. However, similar to RF phase shifting via TDDs, this technique is only capable of sensing a single spatial direction at a time. Further, in the context of wideband beamforming, the design of high frequency LOs with wide tuning range while marinating fine and synchronized phase shifts between LOs is daunting. Consequently, control of the center frequency and phase shifts over a wide span of frequencies is achieved only at the expense of spectral purity at the local oscillator.

2.2. Digital Beamformer

The aforementioned pitfalls motivate the move towards digital beamforming. In this case, the RF signal is processed and digitized prior to phase-shifting at digital stage. That is, the RF front-end now performs only the signal reception (as shown in Fig. 4). Of course, the received range of frequencies is still limited by the receiver bandwidth. This issue is alleviated by using wideband apertures.

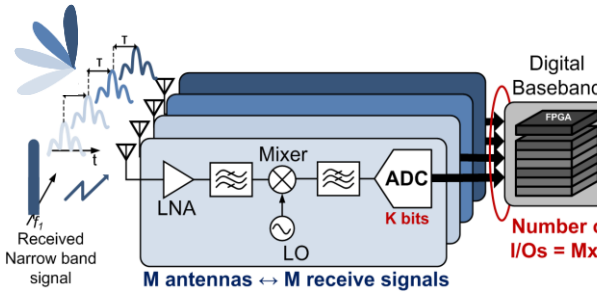

Fig. 4 Digital beamformer using an ADC for each single path.

Digital beamforming became attractive with the realization of software radio (SR) technology. That is, for SR, it is desired to push digitization further toward the front-

end [4]. This offers more flexibility since various algorithms can be tested without hardware modifications. Further, digital adaptive beamformers can achieve more accurate main beams, null steering, control of side lobes levels, simultaneous multi-directional beams, and even spatial diversity by means of multiple-input-multiple-output (MIMO) systems [1].

Still, existing digital beamformers at baseband have extensive hardware requirements as they employ separate ADCs for each signal path as shown in Fig. 4. The large number of high cost and power hungry ADCs results in excessive power consumption in the back-end circuitry, making such approaches limited to small arrays. For instance, an M-element array requires M-ADCs with k-bits resolution. Therefore, a FPGA with $M \times k$ parallel I/O channels is required that does not exist in the market. As a result, multiple or an array of FPGAs is needed implying even more even more daunting design challenges (power and size overhead, synchronization, etc...).

3. DIGITAL BEAMFORMER WITH ON-SITE CODING

In an effort to achieve a significant size, weight, area, power, and cost (SWAP-C) reduction, herewith, we first propose to combine all array elements paths into a single ADC, as illustrated in Fig. 5. The issue then to overcome is a way to afterwards separate the combined antenna elements signals.

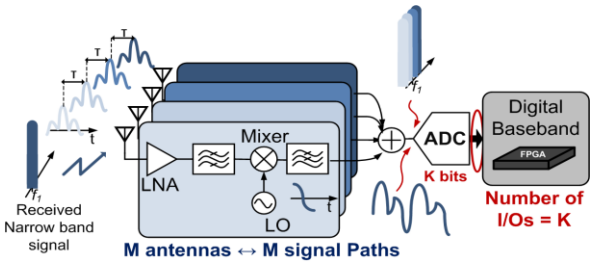

Fig. 5 Digital beamformer with hardware sharing.

To separate out the combined array signals after digitization, in this paper we introduce an on-site code division multiplexing (CDM) technique. This is a key innovation of our beamformer and guarantees the faithful recovery of the signal at digital baseband. As shown in Fig. 6, each analog signal $s_i(t)$ of bandwidth B is modulated at IF with a unique orthogonal spread spectrum code $c_i(t)$ of length L_c and chip rate R_C. Typically, R_C is much greater than B, and more precisely, $R_C = B \times L_c$ (L_c is usually referred to as the processing gain or spreading factor). The bandwidth of resulting spread signal $s_i(t) \times c_i(t)$ becomes then equal to the chip rate. Subsequently, all received signals from the M-antenna elements are summed into a composite signal as

$$s_{sum}(t) = \sum_{M} s_i(t) \times c_i(t) \qquad (2)$$

without loss of identity.

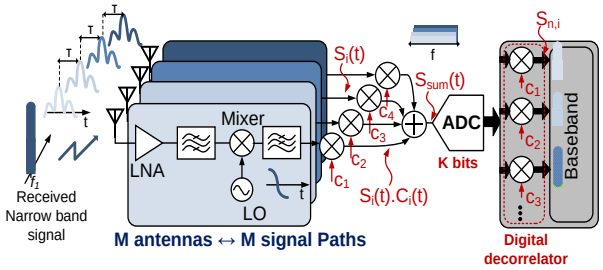

Fig. 6. Proposed digital beamformer with on-site coding and a single ADC for receiving multiple narrowband signals across large bands

The summed received signal $s_{sum}(t)$ can then be processed through a single high speed ADC for digitization. To satisfy the Nyquist criterion, the ADC bandwidth should be at least twice the spread signal bandwidth [6]. That is, assuming a k-bit resolution ADC, the output bit stream $s_{n,sum}[k]$ (n is the number of samples), is decorrelated with the same spreading codes c_i. The signal attributed to each of the array elements is then recovered in digital form, as $s_{n,i}[k]$. At this stage, all digital signals are supplied to FPGA for further processing including beamforming and cognitive functions using multiple beams.

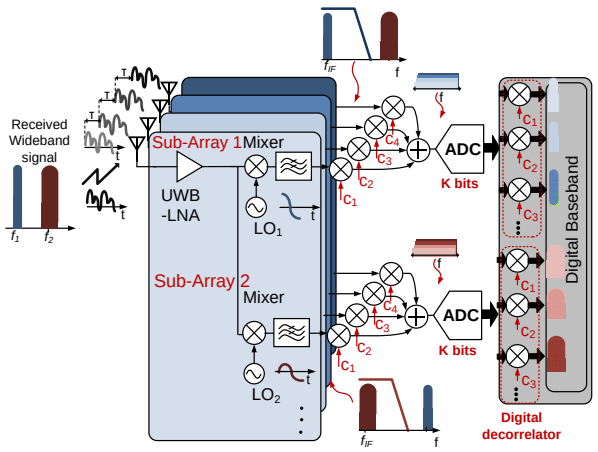

Fig. 7 Channelized receiver for UWB reception.

4. UWB DIGITAL BEAMFORMER

The design of UWB digital beamformers necessitates the apertures capable of sensing UWB signals (more than 20:1 impedance bandwidth [7,8,9,10]). This bandwidth allow for processing multiple narrowband signals concurrently as they illuminate the aperture at different angles and become

spectrally multiplexed into a compound UWB signal. Such receiver is illustrated in Fig. 6. Limitations imposed by this receiver are only associated with the bandwidth of the LNAs, mixers, and ADCs.

The issue of large bandwidth LNAs, mixers and ADCs can be circumvented using a channelized UWB receiver [11, 12]. Doing so, an UWB LNA is first embedded behind each array element. Next, as depicted in Fig.7, the UWB signal is channelized into multiple narrow sub-bands. This is possible by employing a bank of mixers with the appropriate LOs and low pass filters (LPF), obviating the need for bandpass filters. Here, to guarantee full signal recovery at digital baseband for each sub-channel, code division multiplexing (CDM) is carried right after mixing. The resulting composite signal is then processed by a single ADC. As an example, for an UWB receiver composed of M antenna elements and N frequency bands, our proposed receiver requires M LNAs, M×N mixers and LPFs and N ADCs. Compared to traditional channelized receiver, we are able to decrease the number of ADCs by a factor of M.

5. PROPOSED SYSTEM EVALUATION

Referring to Fig. 7, for an M-element array, each sub-array includes up to M signal paths, ultimately combined to form the input to a single ADC. Prior to combining the signals of each sub-array, each antenna's signal is encoded using a code having a spreading factor L_c. Hence, the maximum number of signal paths that can be aggregated into a single ADC, denoted by N_c, should at most be equal to L_c. In case $N_c < M$, the sub-array is divided into multiple clusters, each including up to N_c signal paths and served by a single ADC (see Fig. 8). The maximum number of clusters per sub-channel is then $C = M/N_c$.

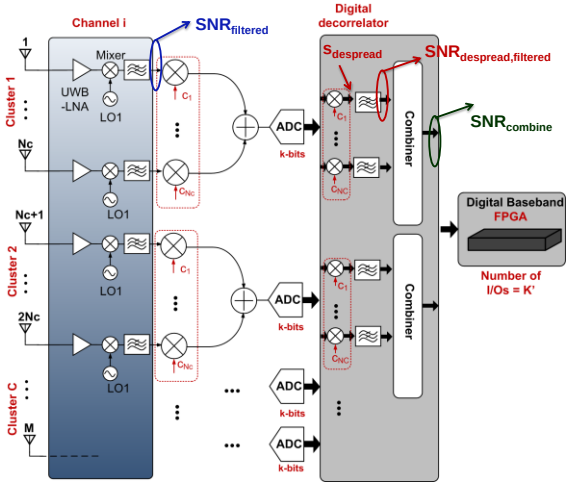

Fig. 8 Channel clustering to relax the ADC speed requirements due to spread spectrum coding.

A higher spreading factor L_c implies bigger clusters, but also requires higher speed ADCs. Therefore, it is essential to limit the number of combined signals based on the cost versus speed associated with the ADCs. In this regard, it is important to note that the maximum signal bandwidth is typically 20-50 MHz. Keeping this in mind, we can greatly relax the cost and the power requirements, and significantly reduces the overall size of the whole system (see Table I). For instance, considering two sub-channels and a cluster size of 8 signal paths, the total number of I/O pins required for the proposed system is 160, i.e., 8 times less than the number of pins required in conventional digital beamformer architecture.

Table I. Illustrated Size reduction due to optimal utilization of ADCs, wiring, and number of FPGA I/O pins.

No. of antennas (M)	No. of SS codes (N_c)	No. of Clusters (C)	No. of sub-channels	No. of ADCs k = 10bits	FPGA I/Os pins
Conventional	-	M	S	M×S	M×S×k
64	-	64	2	128	1280
Proposed	L_c	C = M/N_c	S	C×S	C×S×k
64	8	8	2	8x2=16	160

6. SIMULATION RESULTS

To evaluate the recovered signal quality at baseband and expected signal-to-noise ratio, simulations were performed using MATLAB and verified via AWR Microwave Office (MWO) software. For this, we assumed a cluster of 8 elements using a pool of Walsh codes having a spreading factor 16. The transmitted signal is a 500 MHz carrier modulated using the binary phase shift keying scheme (BPSK) with a 50 MHz bandwidth. Once this signal is down-converted to baseband (LO at 500 MHz), and after going through the LPF, the phase shifts are transformed into amplitude scaling. The baseband signal is then spread using Walsh codes and combined to a single ADC (see Fig. 9). The combined signal has a bandwidth of approximately 900 MHz. In the digital baseband, the combined signal is decorrelated using the same set of Walsh codes. The resulting amplitude scaling is maintained (see Fig. 9). More importantly, we demonstrate that the original time delay is recovered allowing for direction finding.

To assess the effect of on-site coding on the output signal-to noise ratio (SNR) of the receiver, we introduce white Gaussian noise (AWGN) to the input of each signal path. After down-conversion, the LPF band-limits both the desired signal and the noise. Next, spreading and combining is introduced, and the summed signal becomes:

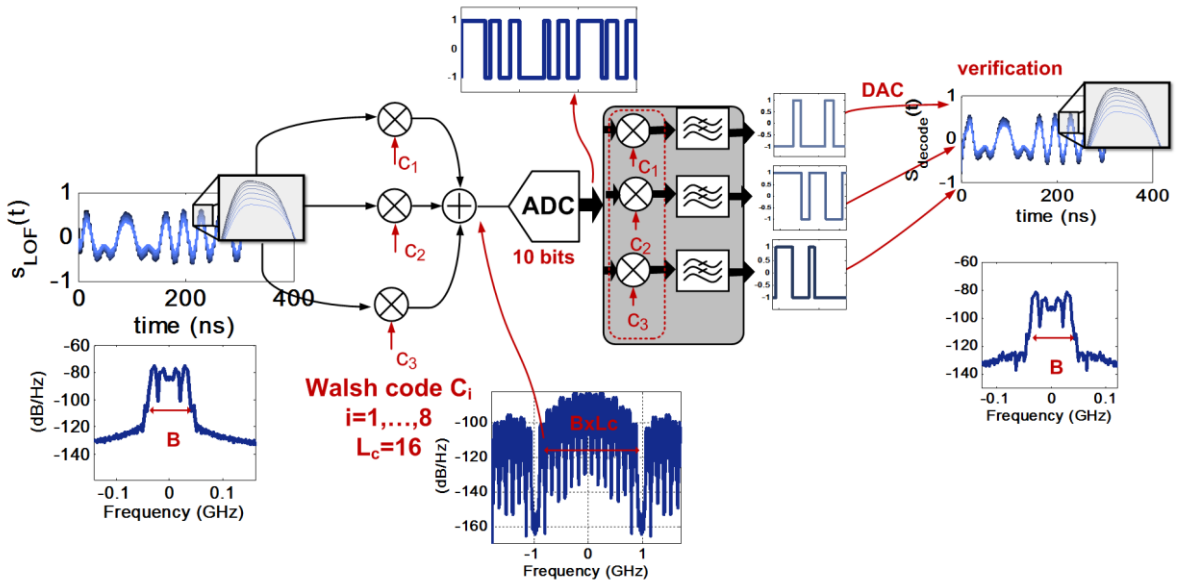

Fig. 9. Illustration of analog spreading and digital de-spreading using a Walsh code of length 8 and a 10-bit resolution ADC. The signals can be faithfully recovered in the digital baseband.

$$s_{sum} = \sum_{i=1}^{8} c_i (s_i + n_i). \tag{3}$$

In the above equation, s_i and n_i are respectively the filtered signal and noise of the i^{th} path right before mixing with the spreading code c_i. Subsequently, after digitization and despreading the signal, we have

$$\begin{aligned} s_{i,despread} &= s_i + \sum_{j=1\neq i}^{8} c_i c_j s_j + \sum_{j=1}^{8} c_i c_j n_j \\ &= s_i + I + N\,. \end{aligned} \tag{4}$$

This is the decorrelated signal referring to the i^{th} path. It shows that the signal contains an interference term I and a noise term N. These terms are due to non-ideal LPF used after despreading. Although Walsh codes are known to be perfectly orthogonal, however orthogonality is only achieved when a brick wall filter is applied right after despreading, which is impractical for real applications. Consequently, the SNR after despreading and low pass filtering is computed as

$$SNR_{despread,filtered} = P_S / (P_I + P_N) \tag{5}$$

where P_s, P_I, and P_N are the decorrelated filtered signal power, the residual inter-channel interference power, and the noise power, respectively. Note that P_N incorporates the noise power of the signal path as well as the inter-channel noise interference power from the other signal paths. The main objective here is to properly design the LPF so to minimize both the co-channel signal and noise interference.

Ultimately, we need $SNR_{despread,filtered} \approx SNR_{filtered}$ (Refer to Fig. 9).

To compute the power (P_I) of the interference term I in (4), we first run the simulation without added noise. By designing a high order (greater than 4) digital LPF implemented after despreading, the difference between the despread signal power and the filtered signal power before spreading is as low as 0.4 dB. Next, to compute the noise power hit (P_N), we shut down the signal and fed the receiver with noise only. In this case, using the same LPF, we observed that the total noise interference has increased to 1.4 dB after despreading and filtering. Therefore, a total of 1.8 dB interference noise increase is expected. Fig. 10 compares the SNR before spreading and after despreading and filtering. More specifically, the filtered SNR before spreading turns out to be 12 dB. On the other, the SNR after despreading and filtering is 12-1.8=10.8 dB.

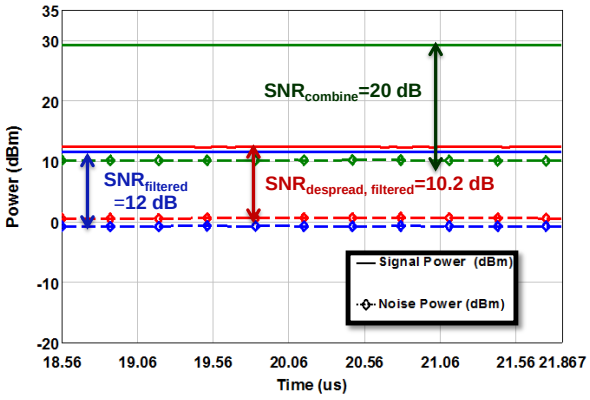

Fig. 10. Signal and noise before and after despreading and filtering, and after digital combining.

From Fig. 10, we found that the slight degradation in SNR is compensated by combining signals in the digital baseband. Referring to Fig. 8, after despreading and filtering, appropriate phase shifting is applied to the signals. At this stage, since signals are correlated (while noise is uncorrelated), by simply combining the signals together, a combining gain can be achieved. Ideally, for an M -element phased array, the combined signal power is increased by a factor of M^2 while the combined noise power is just increased by M. Therefore, the $SNR_{combine}$ is expected to be M times higher than the $SNR_{filtered}$ (see Fig. 8 and 10). Hence, a total of $10log_{10}M$ combining gain can be realized. For our simulation, around 8 dB of combining gain was realized with 8 signal paths compared to the ideal case of 9 dB.

7. CONCLUSION

We proposed a novel reduced hardware transceiver architecture with on-site coding. The proposed system offers a significant reduction in the number of ADCs, and hence, less I/O pins required for the digital modules (FPGA). This approach greatly relaxes cost and power requirements, but even more importantly, significantly reduces the overall size of the whole system. Therefore, digital beamforming for large arrays with concurrent multiple beams can be realized in a practical manner. The proposed system was successfully simulated and preliminary simulations demonstrated the faithful recovery of the signal with a minor degradation of 1.8 dB in SNR. This was compensated for by combining the signals in digital baseband resulting in an 8 dB combining gain.

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