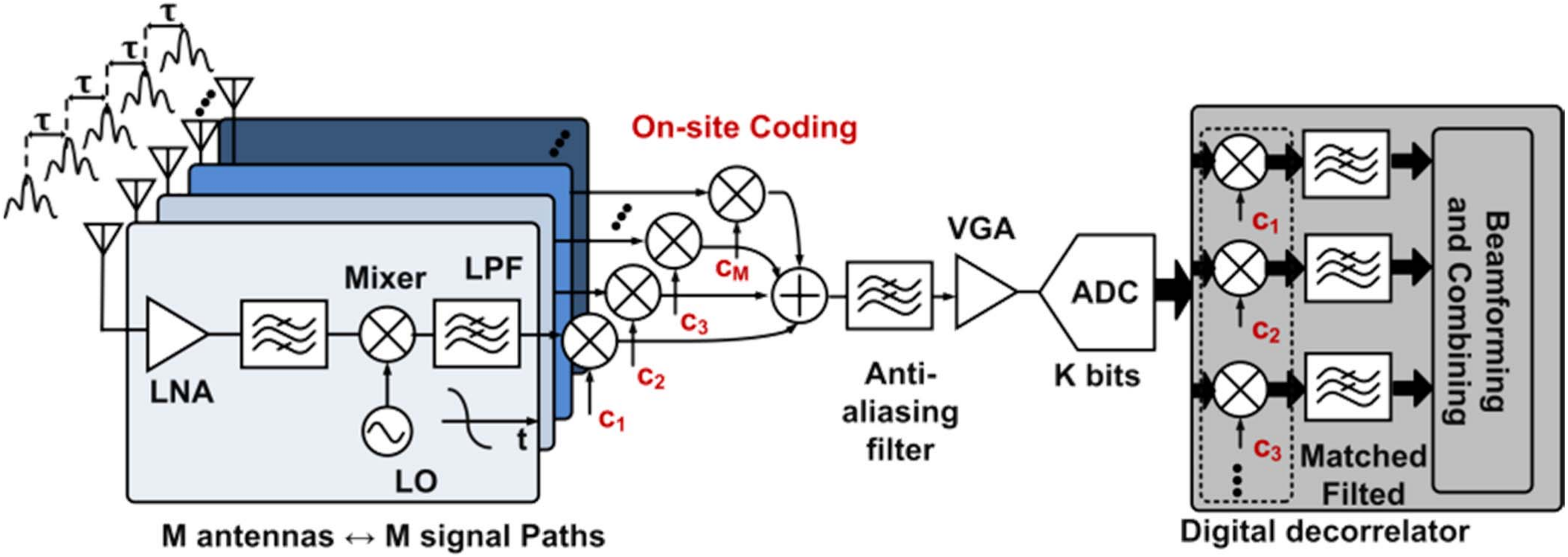
Ultra-wideband Digital Beamformer with Significant SWAP-C Reduction



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Outline

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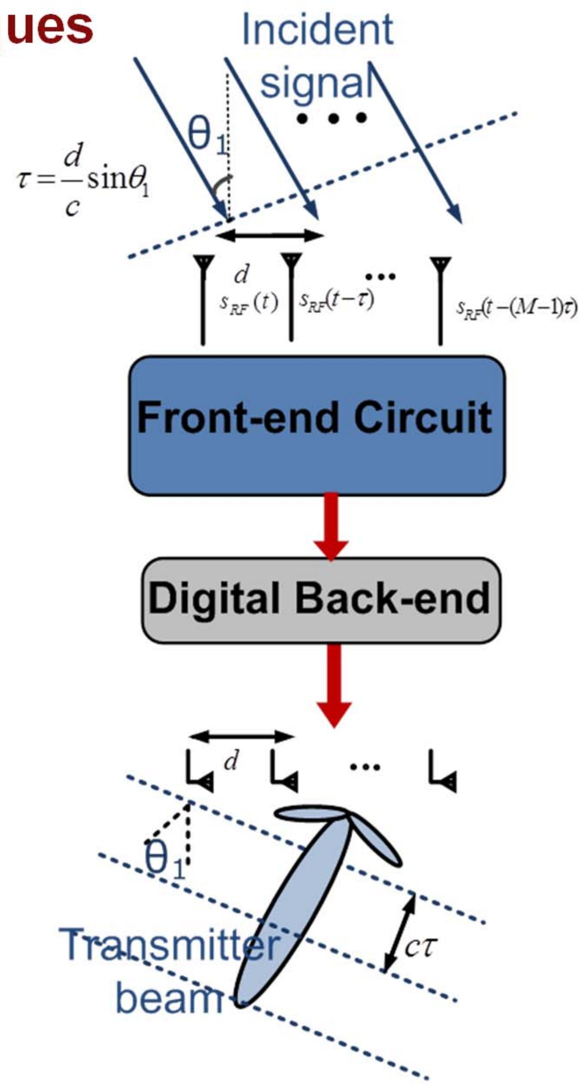
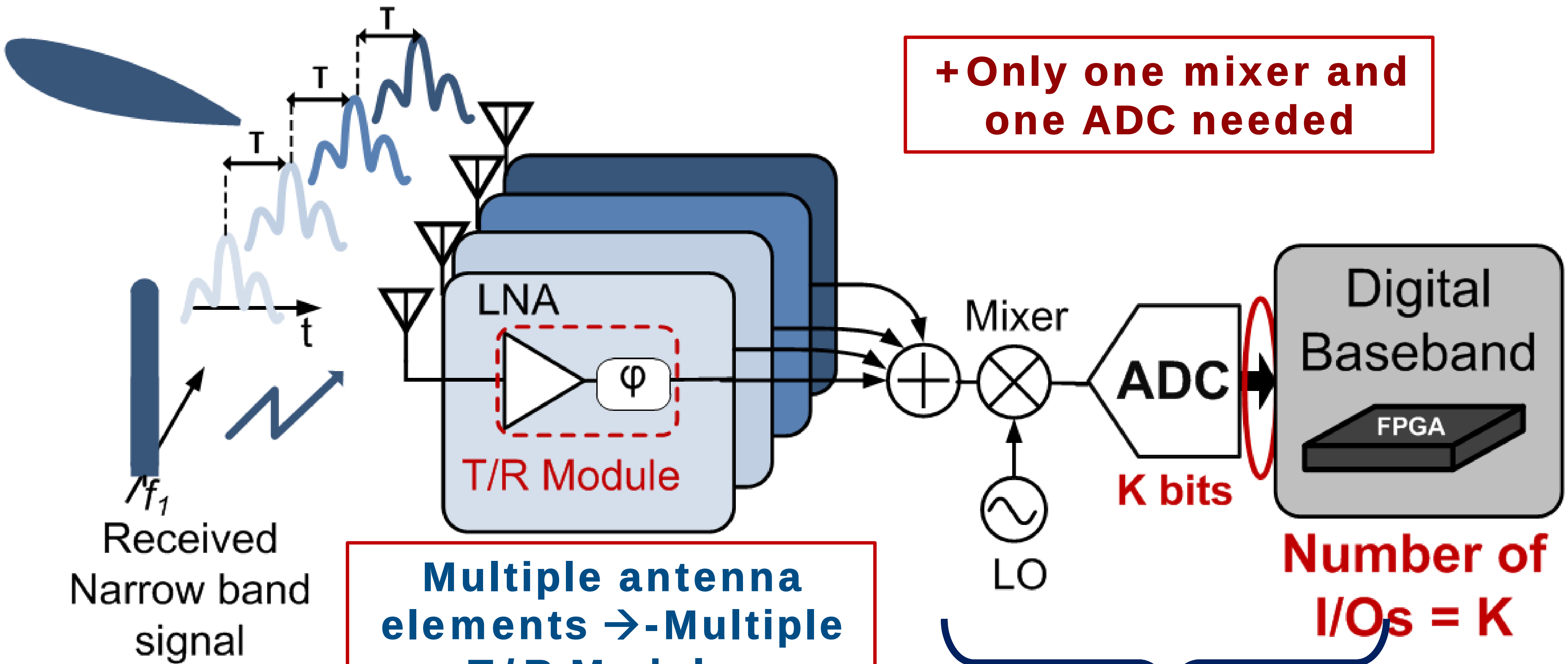
→Analog (RF,LO)
→Digital
2- Proposed On-site coding Receiver (OSCR)
→ Receiver Architecture
3- System Evaluation
- → Size
- → Cost
- → Power

4- System Considerations
→ SINR calculations
→ Type of spreading codes:
- → Orthogonal vs. non-orthogonal codes
- → Code spreading Factor vs. ADC speed
- → ADC quantization noise
- → Low pass filter

5- Future Work and Conclusion



Motivation: Analog Beamformer Architecture At Signal Path (RF)



+Only one mixer and one ADC needed

Multiple antenna elements →-Multiple T/R Modules

At Signal Path:

1-Wideband signals →True -Time delay elements: Amplitude and phase shifters

2-Narrowband signals→ Phase shifters

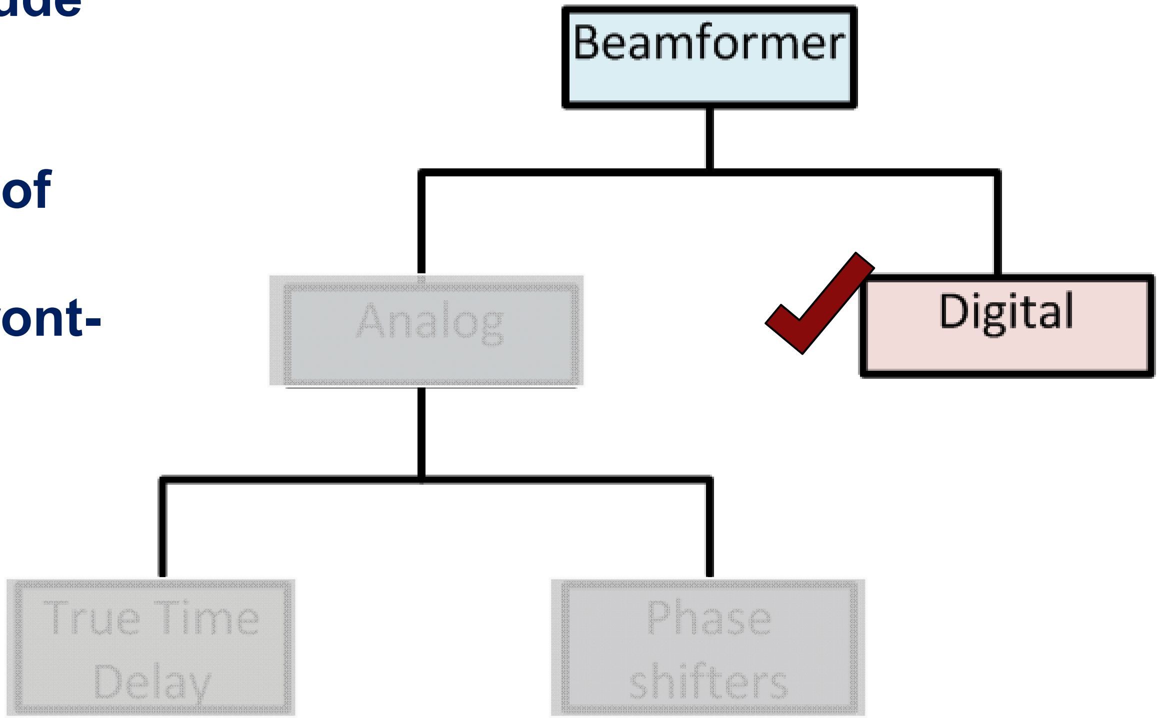
+ Single ADC

- **Only 1 spatial direction at a time**
- **Phase shifter: high area/cost/power requirements**

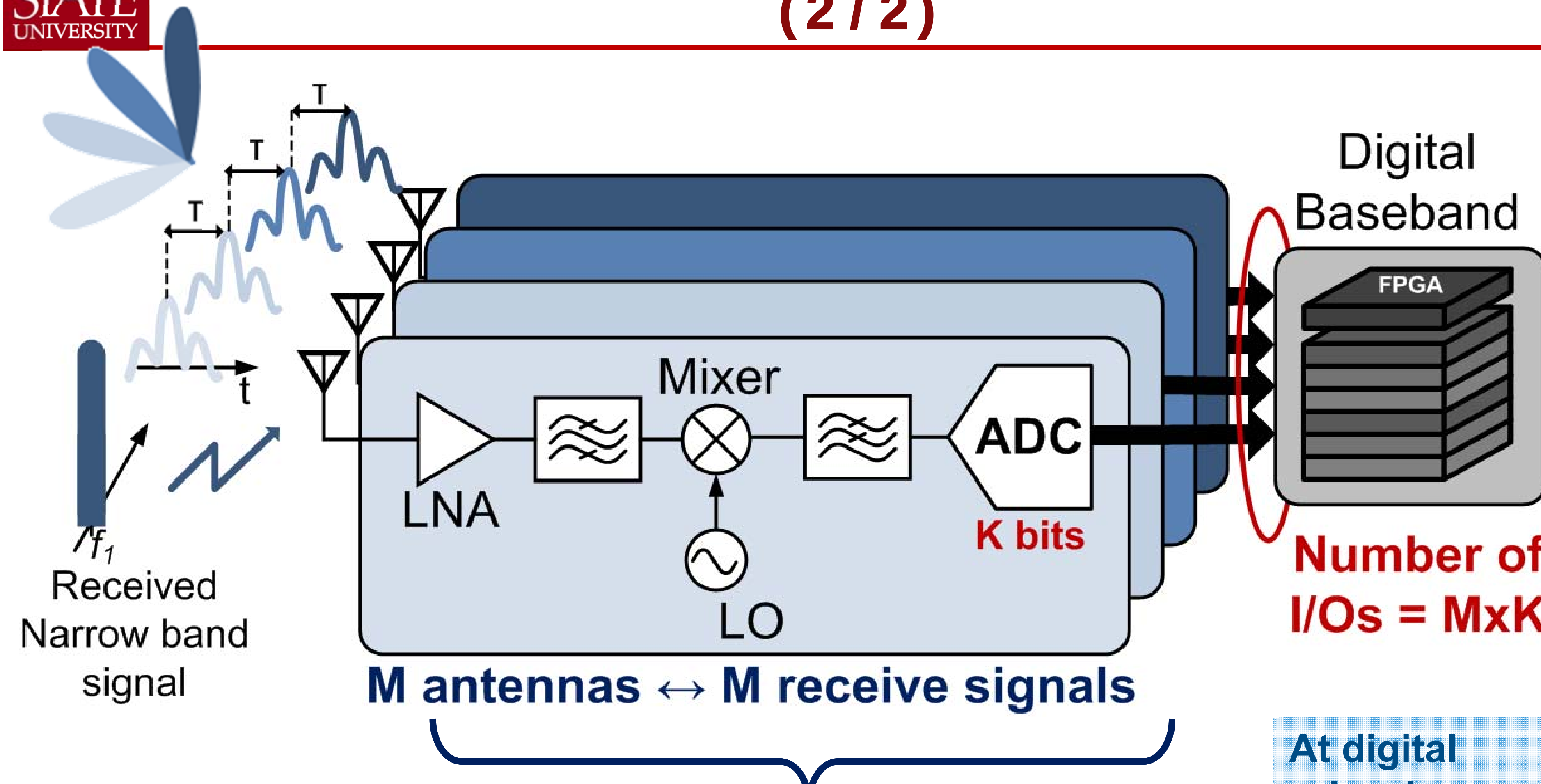
Motivation: Digital Beamformer Limitations (1/2)

Digital Beamformers

- → Phase shifting and amplitude scaling applied at digital baseband
- → No need for phase tuning of the VCOs
- → Relaxed hardware at RF front-end
- → More flexibility (algorithms tested without hardware change)
- → Adaptive algorithm (null steering, multi-beam,…
- → Spatial diversity (MIMO)
- → Intensive Hardware Requirements at digital back end (ADCs, FPGA I/O pins…)



Motivation: Digital Beamformer Architecture (2/2)



At digital level:
-Amplitude /phase shifter

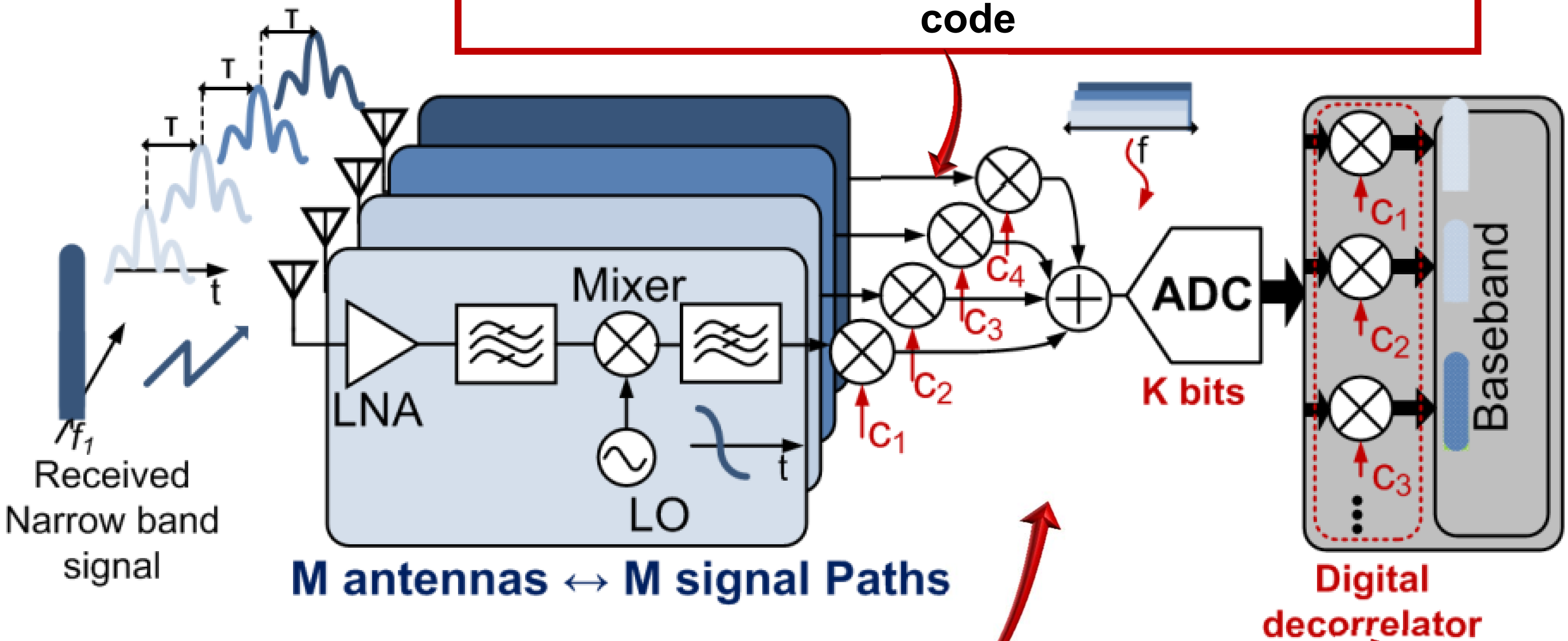
- One ADC per channel: M antennas→ M-ADCs

→ Intense hardware requirements on digital beamforming front-ends (for existing architectures)

Can we share ADCs across multiple channels?

Proposed Digital Beamforming (DBF) technique With On-Site Coding

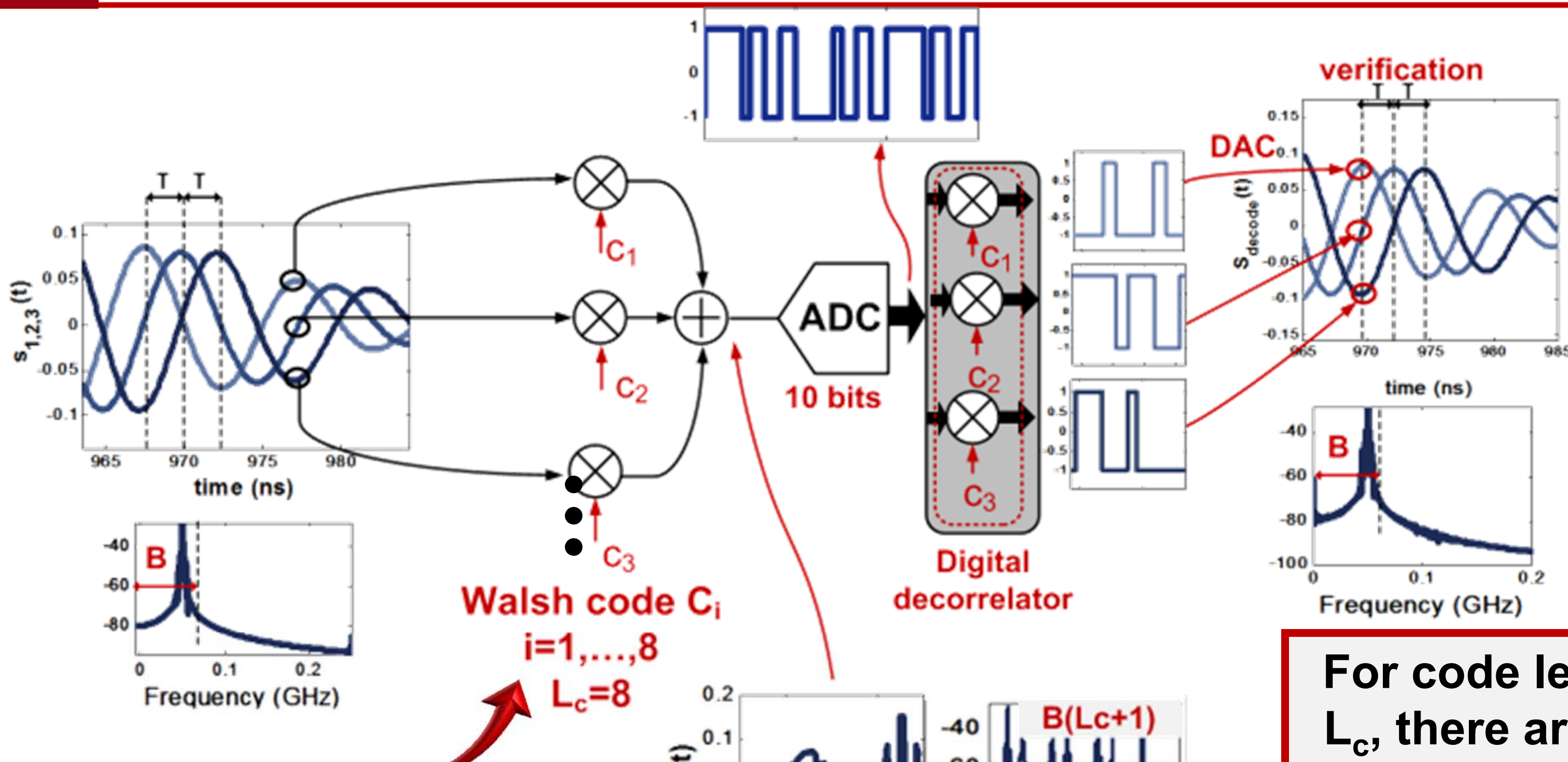
Spread each channel output with an orthogonal code

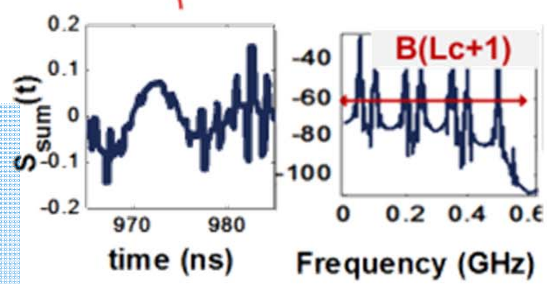


The spreading code serves to uniquely identify each signal path

De-spread the signal digitally: recover

Analog Spreading and Digital Despreading





For code length= L_c, there are max L_c orthogonal codes

Spread Spectrum

- -Direct Sequence: PN sequences, Gold Codes, Walsh Hadamard…
- -Orthogonal Codes:

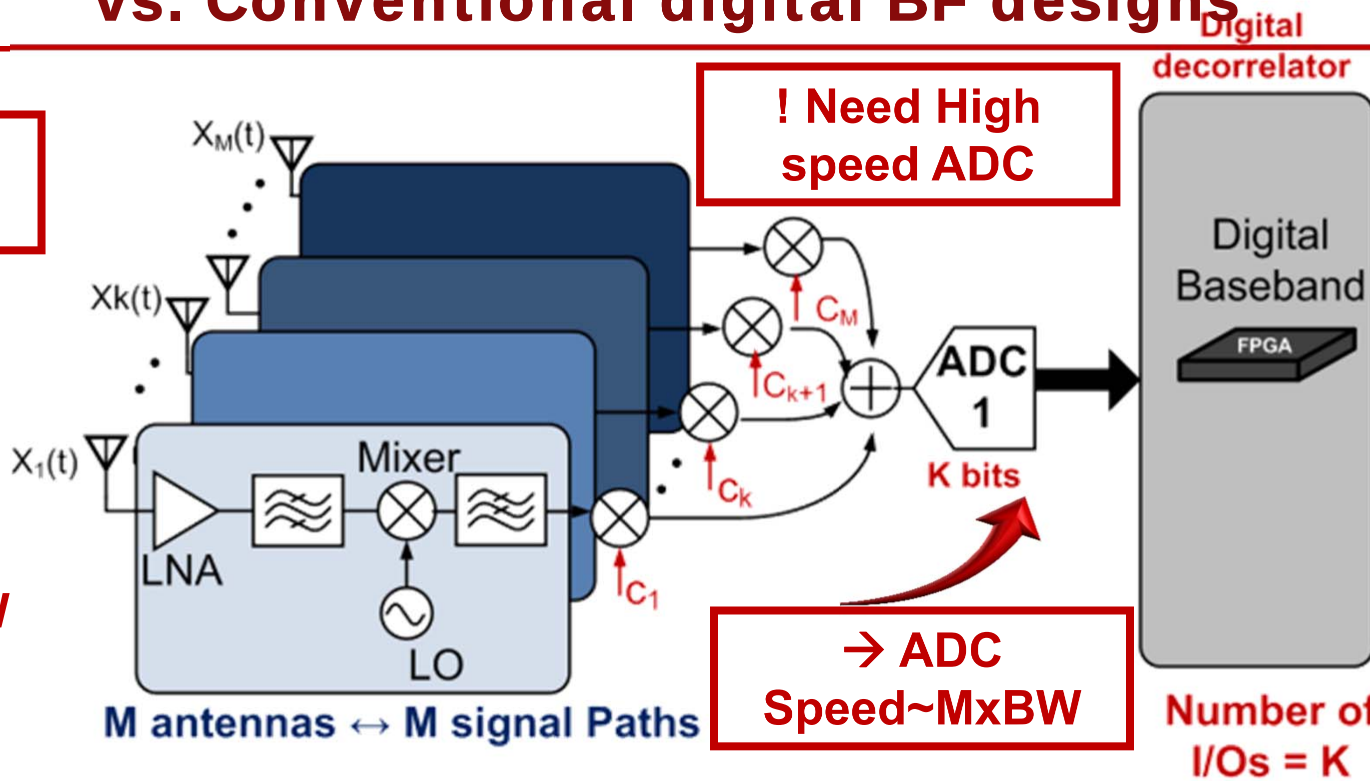
$$\langle c_i | c_j \rangle = \begin{cases} 1, i = j \\ 0, otherwise \end{cases}$$

Combined BW= 2B.Lc
→ ADC Speed=2xBW

Significant Size Reduction of the Proposed vs. Conventional digital BF designs

OSCR: 1
ADC/front end

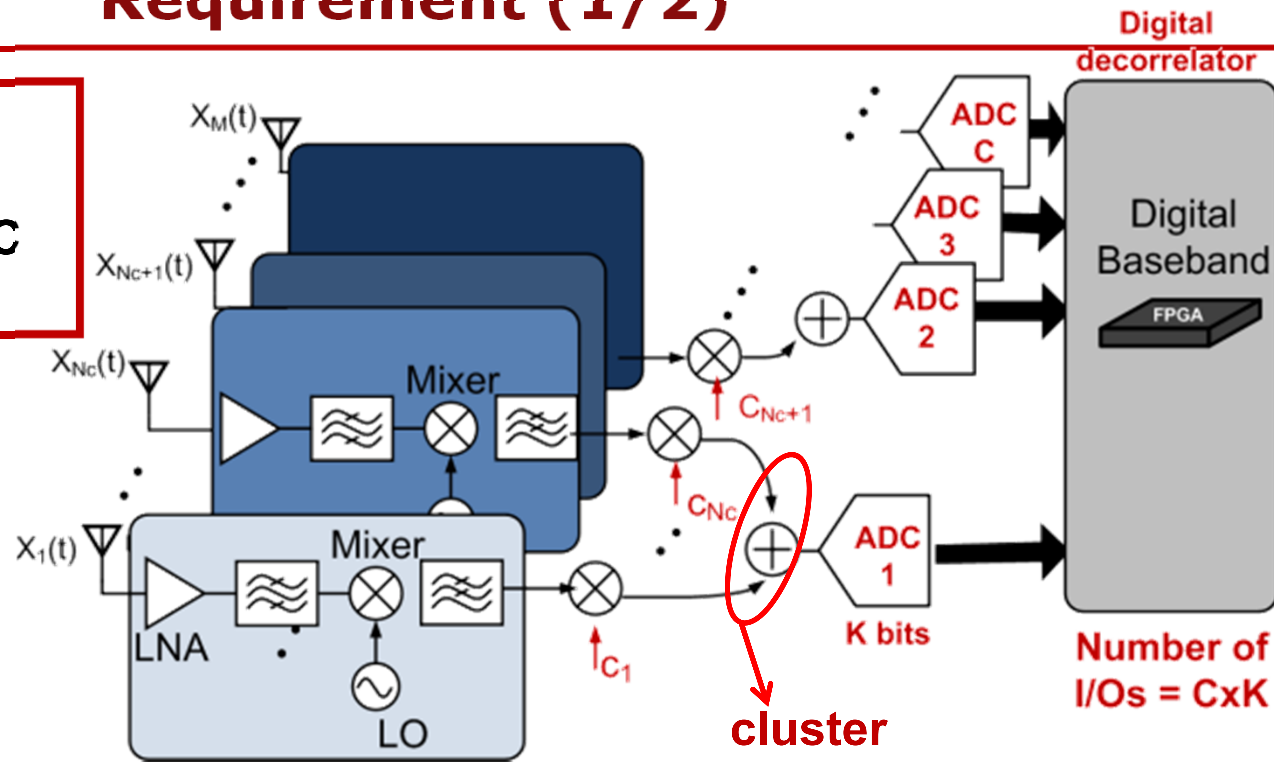
Signal Bandwidth BW



No. of antennas (M)	No. of ADCs k= 10bits	FPGA I/Os pins
Conventional		
64	64	640
Proposed		
64	1	10

OSCR with Clustering to Relax ADC speed Requirement (1/2)

Shared ADC per cluster
→ M signal paths
→ N_c signal paths per ADC
→ $N_c < L_c$ (code length)



→ ADC Speed ~ N_cxBW<<MxBW

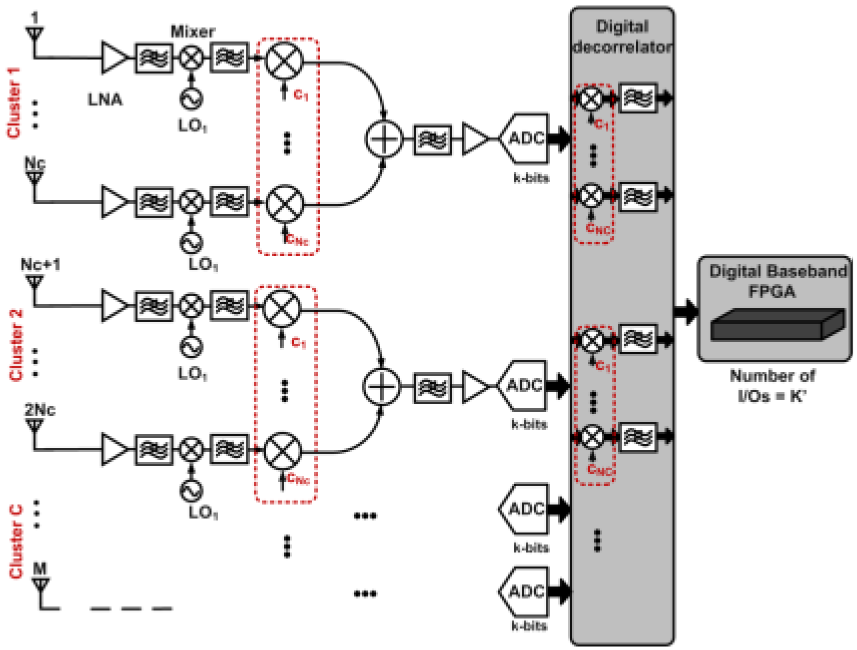
What is the Optimal Cluster size that achieves:
1- minimum hardware requirement
2- low power consumption
3- low cost

Proposed Architecture Cost and Power Requirements (2/2)

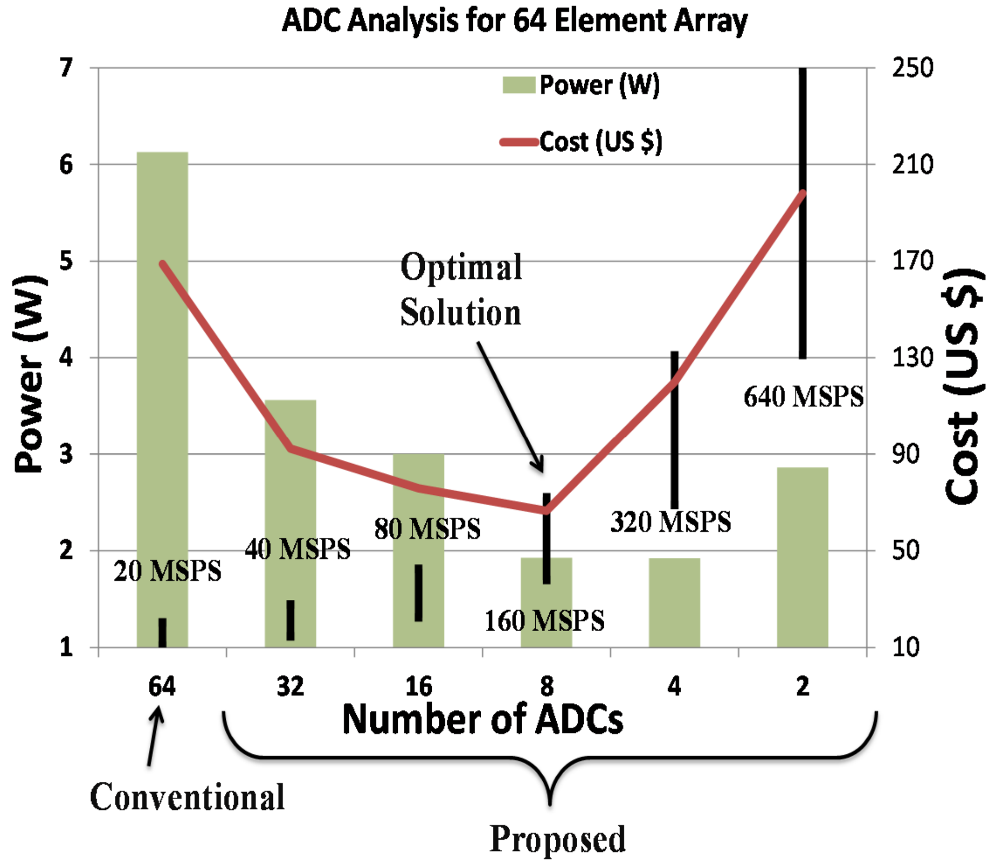
<u>Significant ADC reduction</u>

→power Reduction

→ Cost Reduction



Maximum cluster size C ≤ Maximum number of orthogonal codes of length L_c



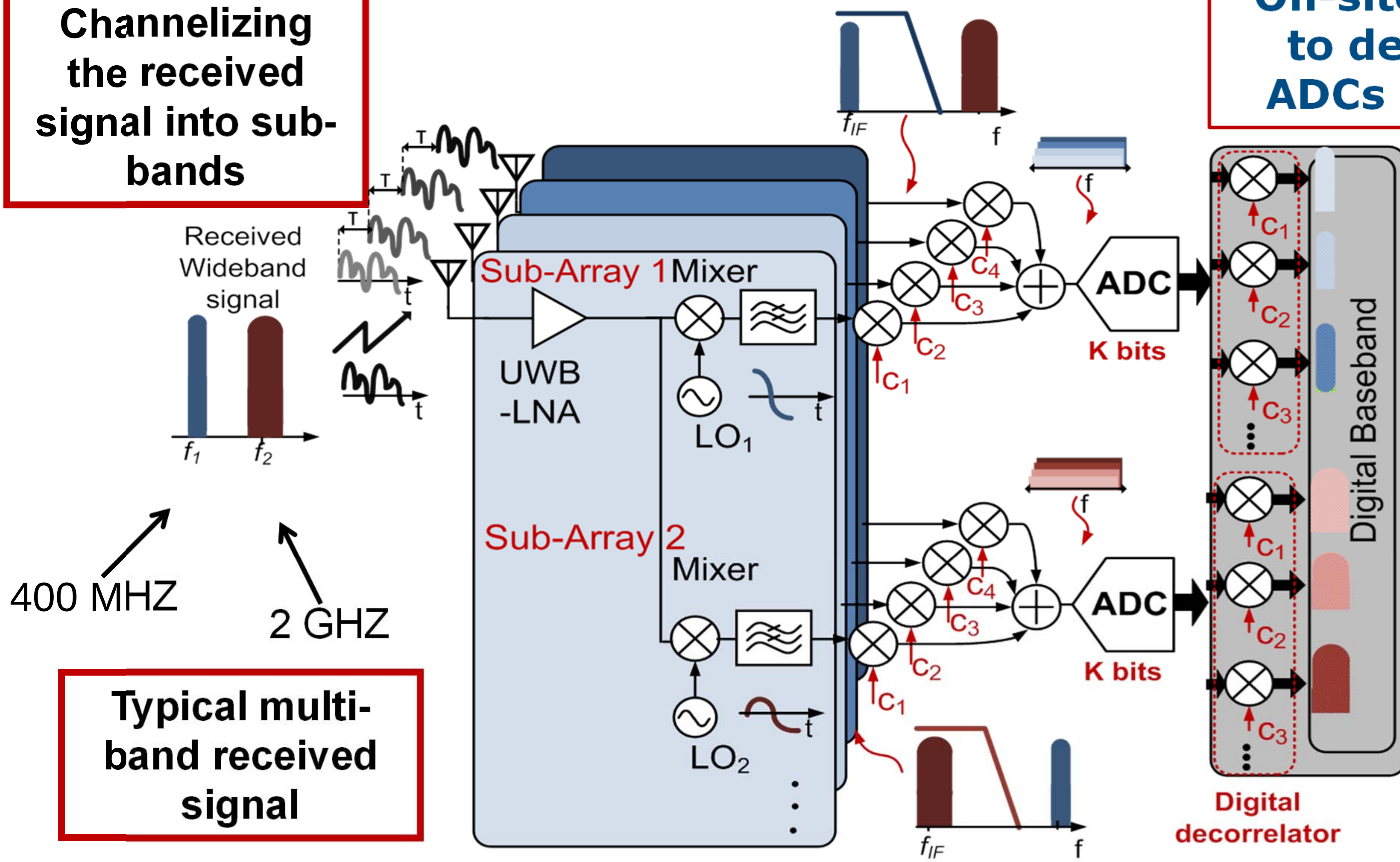
<u>E.g. 64 elements array</u>

Optimal solution→ 8 ADCs each serving 8 signal paths

UWB Receiver with onsite coding

Channelizing the received signal into sub-bands

On-site coding to decrease ADCs number



Typical multi-band received signal

Clustering can be used to relax the ADC speed requirement

System Considerations (1/2) Signal-to-Interference-and-Noise Ratio (SINR)

Assumptions

→Up to N_c signal paths
→Length of code L_c
→ADC: ∞-resolution

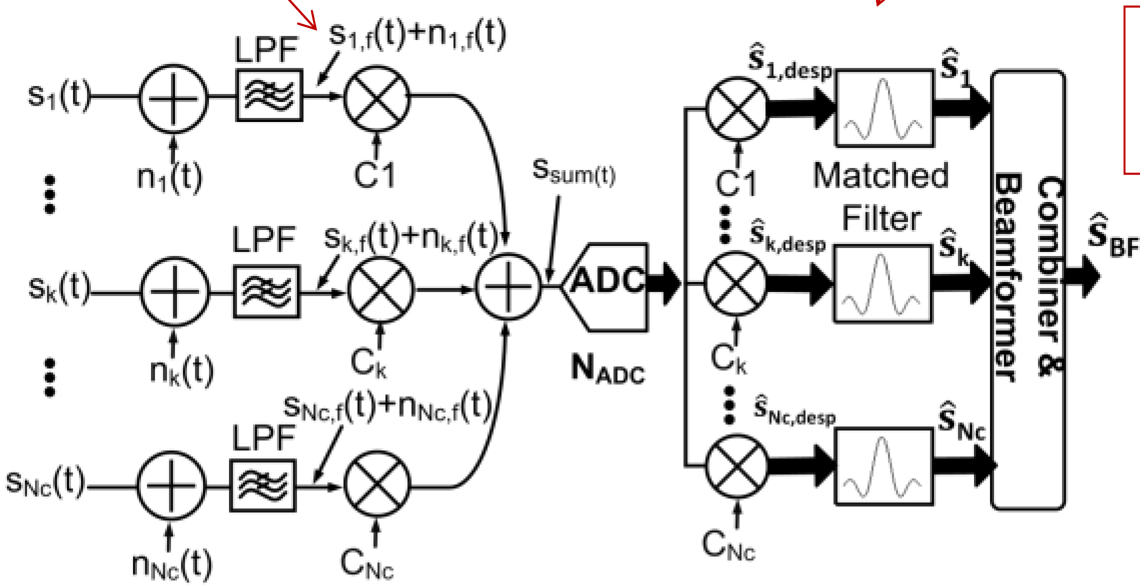
$$SINR_{Input} = \frac{P_{k,f}}{N_{k,f}}, k = 1, \dots Nc$$

Desired signal of path 1

Recovered noise of path 1

$$\hat{s}_{1,\,desp} = s_1(t)c_1(t)c_1(t) + n_1(t)c_1(t)c_1(t) + \sum_{i=2}^{Nc}\left(s_i(t)c_i(t)c_1(t) + ni(t)c_i(t)c_1(t)\right)$$

Inter-channel interference (signal and noise)



$$SINR_{OSCR,\,1} = \frac{P_{1,f}}{\underbrace{C_c^2 \sum_{i=2}^{Nc}\left(P_{i,f} + N_{i,f}\right)}_{} + N_{1,f}} \xrightarrow{C_c \to 0} SINR_{Input}$$

Inter-channel signal and noise Interference:

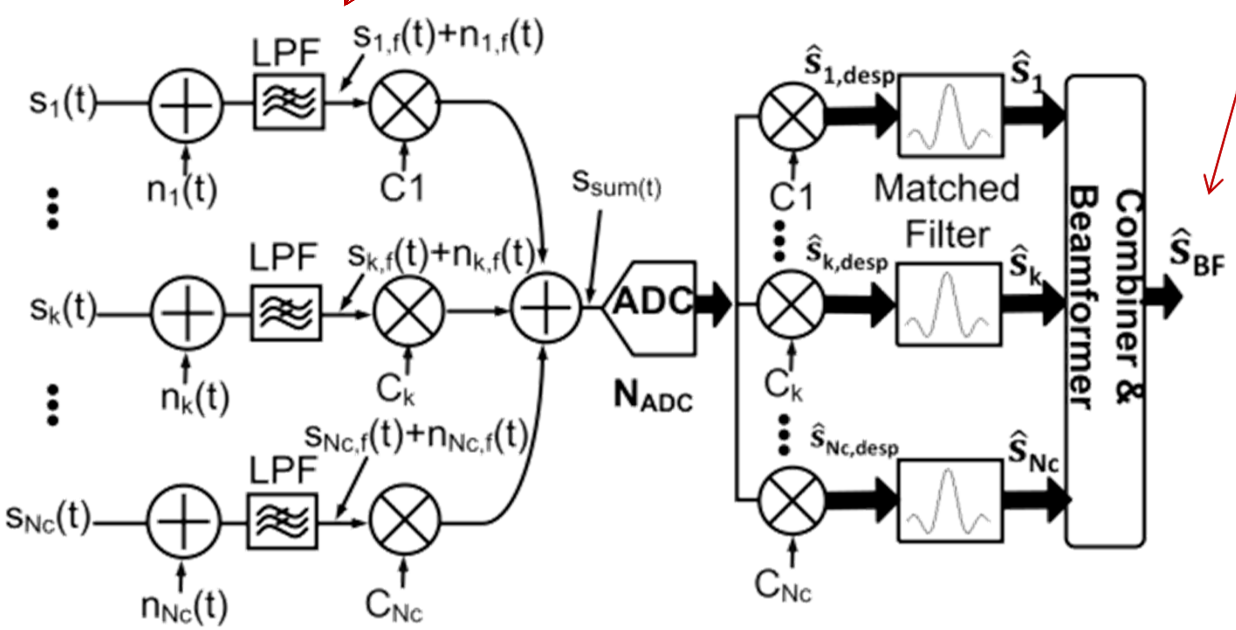
→ Using orthogonal codes: Cross Correlation C_c→0

System Considerations (2/2)
Beamforming Gain

Assumptions
- →Up to N_c signal paths
- →Length of code L_c
- →ADC: ∞-resolution

$$SINR_{OSCR\_BF} = \frac{N_c^2 P_{1,f}}{N_c[C_c^2 \sum_{i=2}^{Nc}(P_{i,f} + N_{i,f}) + N_{1,f}]} \xrightarrow{C_c \to 0} N_c SINR_{Input}$$

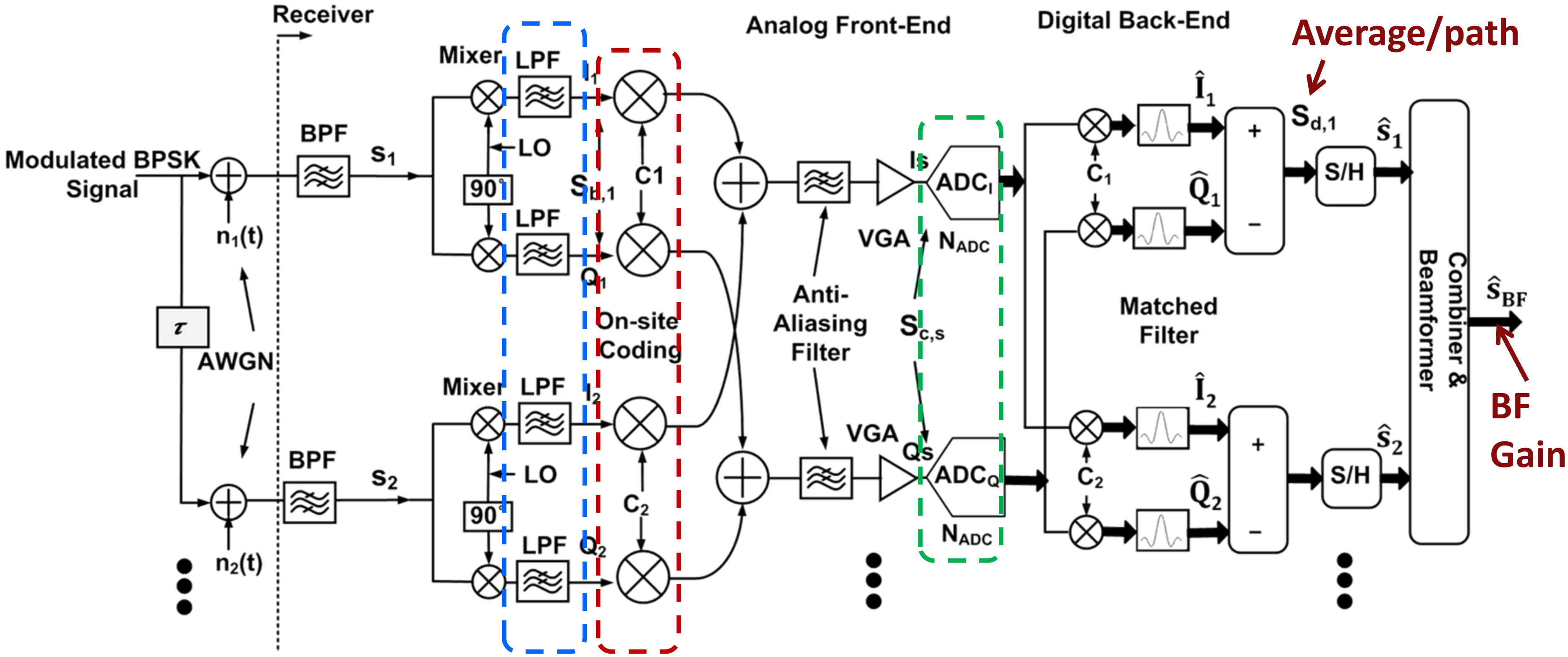
$$SINR_{Input} = \frac{P_{k,f}}{N_{k,f}}, k = 1, \ldots Nc$$



Beamforming Gain

→SNR gain $(\sim 10log_{10}N_c)$ is realized by combining the signals after decorrelation (C_c→0)

Equivalent system model for BER calculations



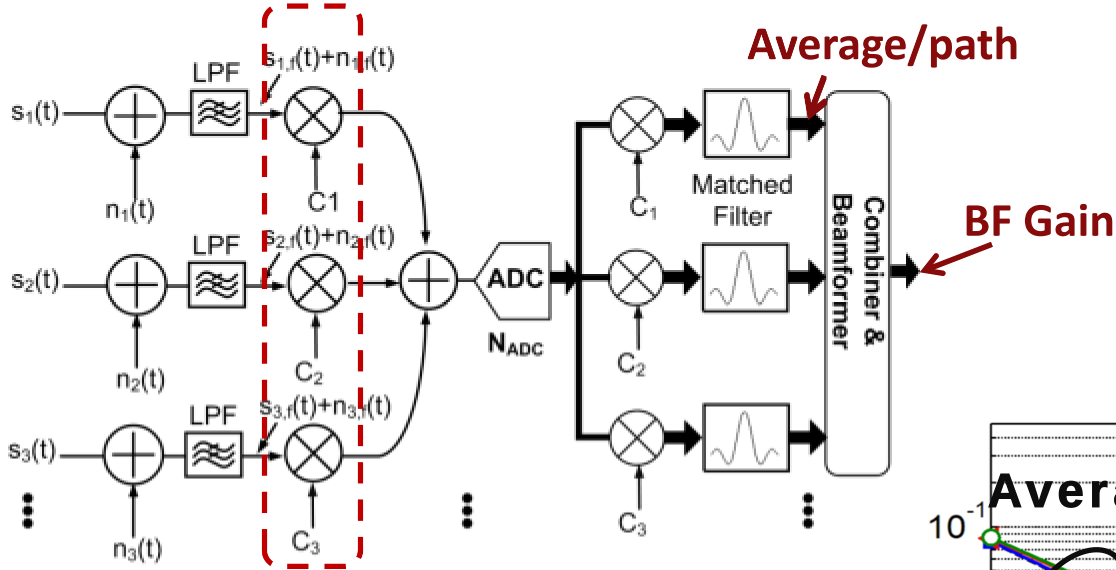
Non-idealities

1- Codes: non-orthogonal codes→ more ICI

2- Low pass filters: more noise in the band of interest

3- ADC quantization noise

BER for 2, 4 , 8 paths using orthogonal codes (Walsh codes) and under ideal conditions



Assumptions

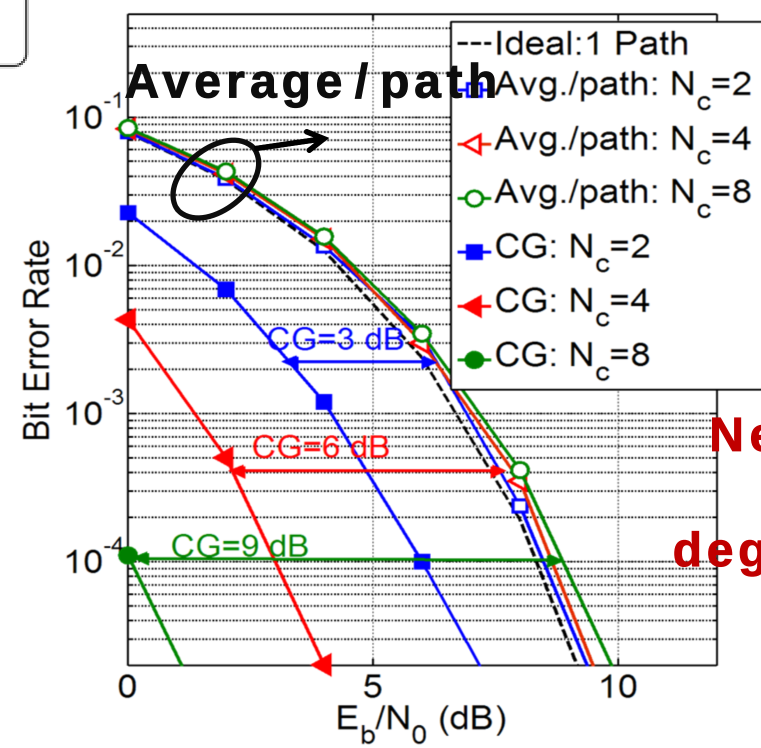
1- Walsh codes

2-length 32

3-Perfectly orthogonal→

C_C=0

4-Nc:# of paths

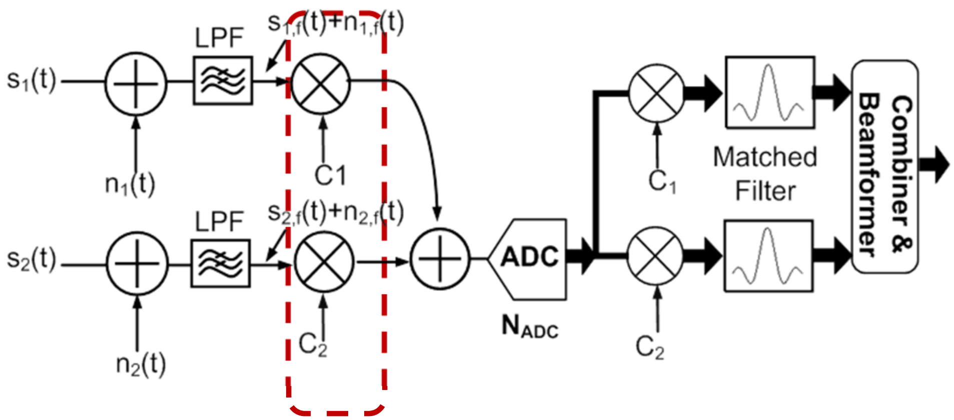


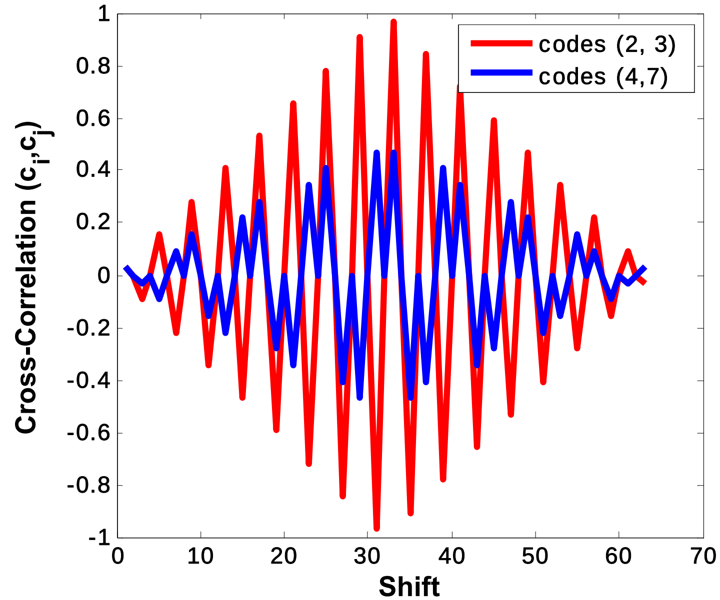
Negligible SNR degradation

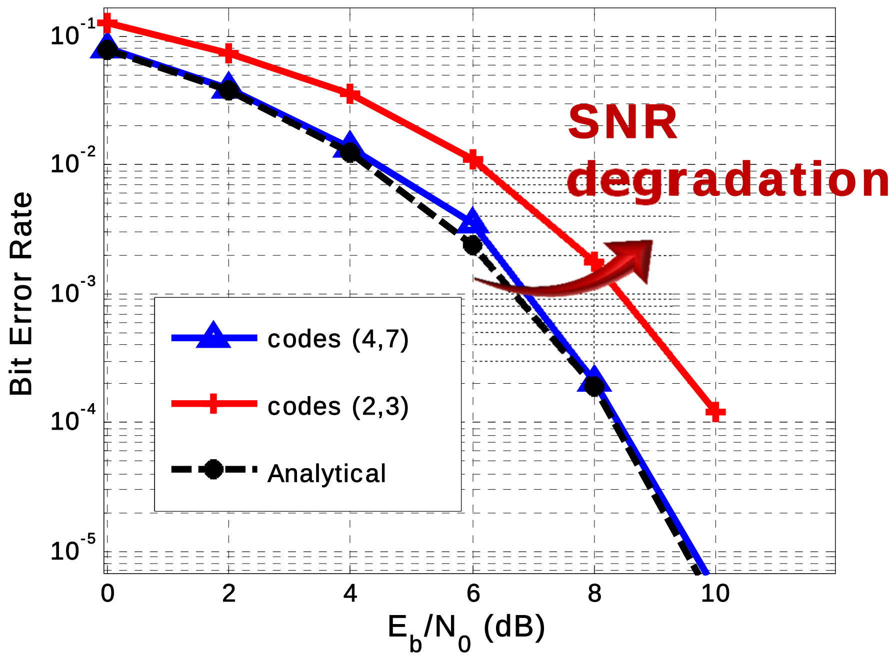
Observations:

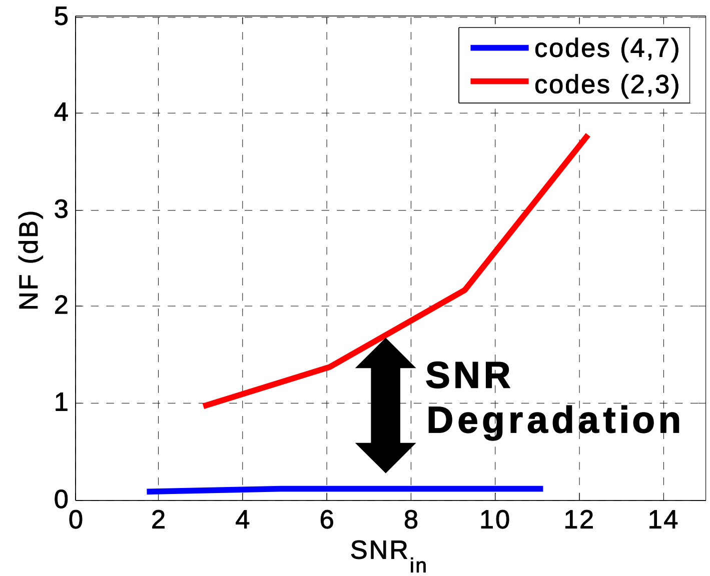
→ Negligible SNR degradation per path

More into NON-orthogonal codes → Walsh Codes, L_c=32, 2 signal paths

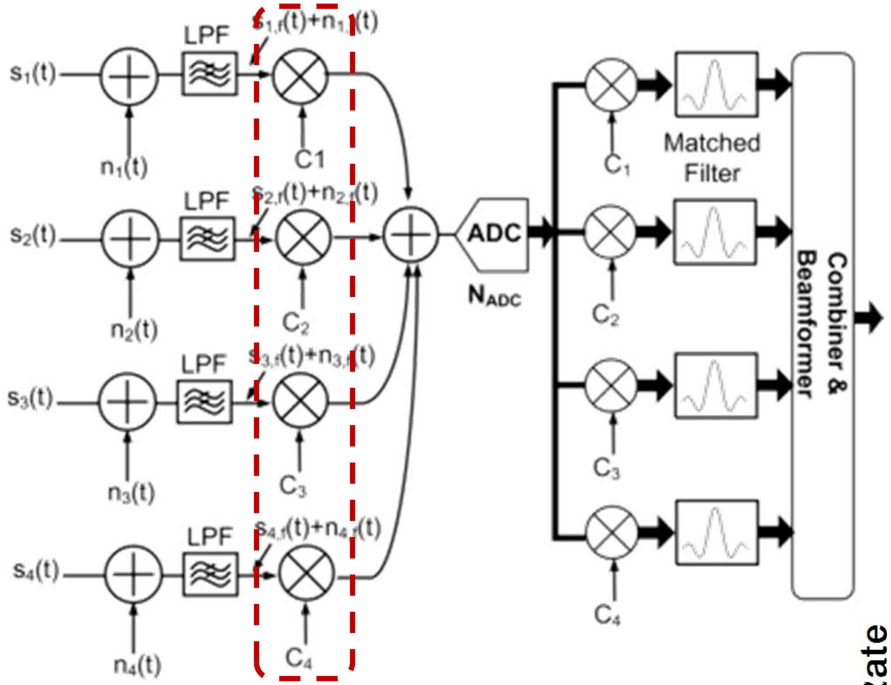








Code-Length Optimization for 4 Antenna Elements Signal Paths



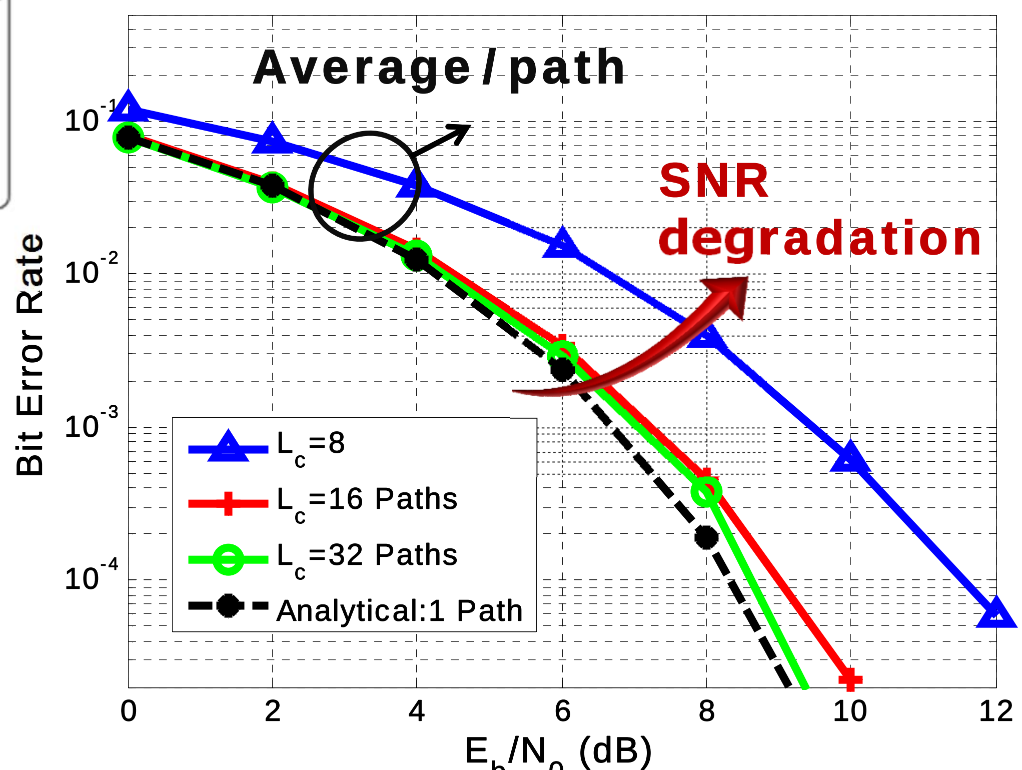
Assumptions

1- Walsh codes

2-length 8-16-32

3-$C_C \neq 0$

4-Nc:4 paths

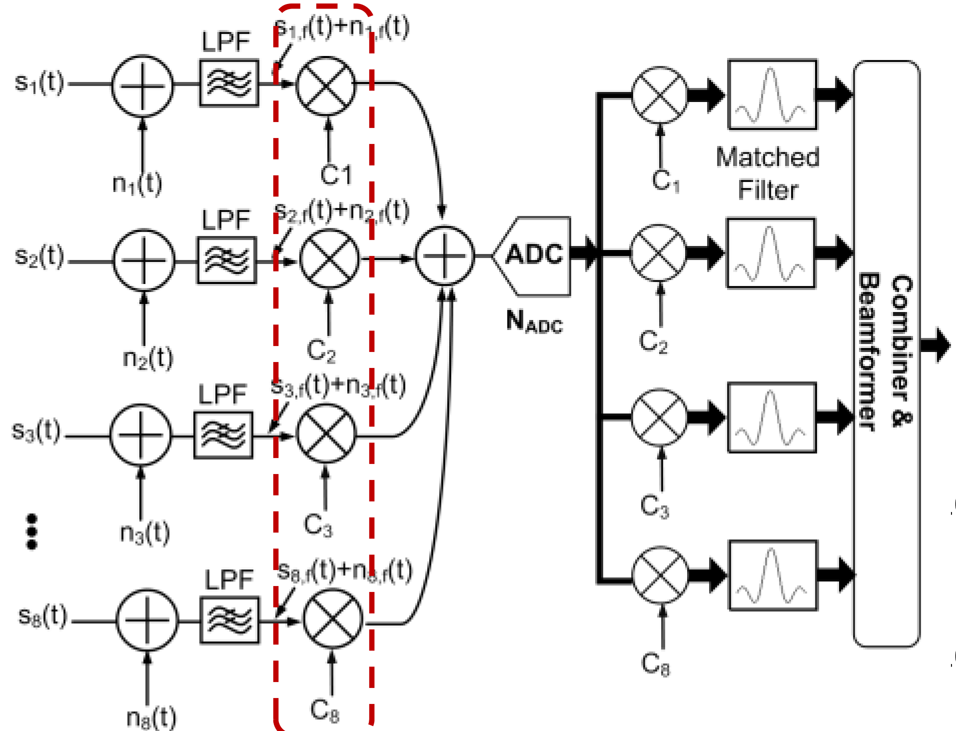


Observations:

→Significant SNR degradation when N_c~L_c/2

→ For a receiver with 4 signal paths, minimum code length Lc>8

Code-Length Optimization for 8 Antenna Elements Signal Paths



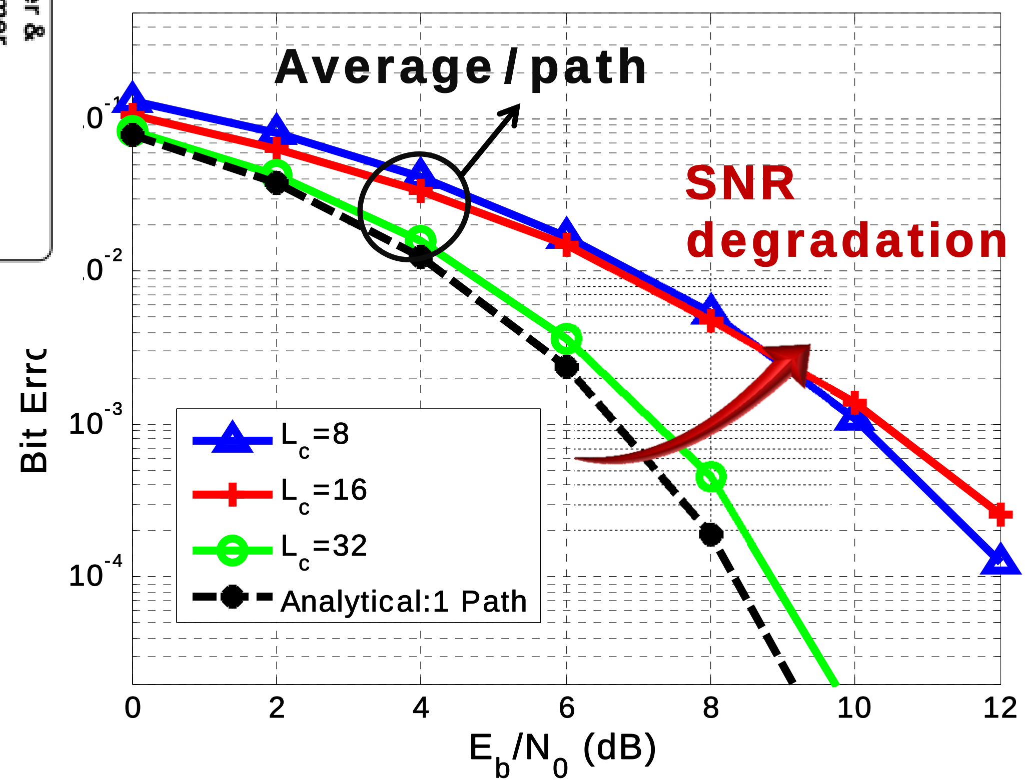
Assumptions

1- Walsh codes

2-length 8-16-32

3-$C_C \neq 0$

4-Nc:8 paths

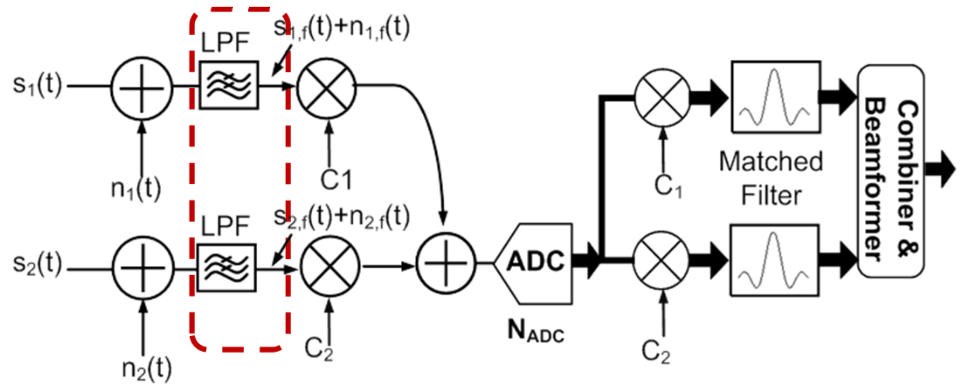


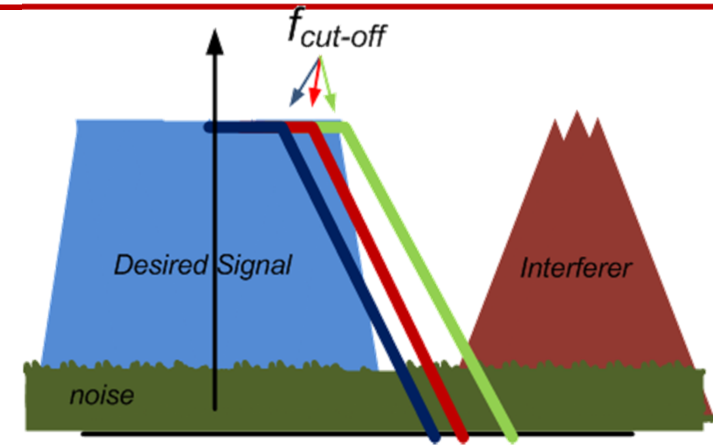
Observations:

→Significant SNR degradation when N_c~$L_c/2$

→ For a receiver with 8 signal paths, minimum code length Lc>16

Effect of the Analog Low Pass Filter on the SNR degradation



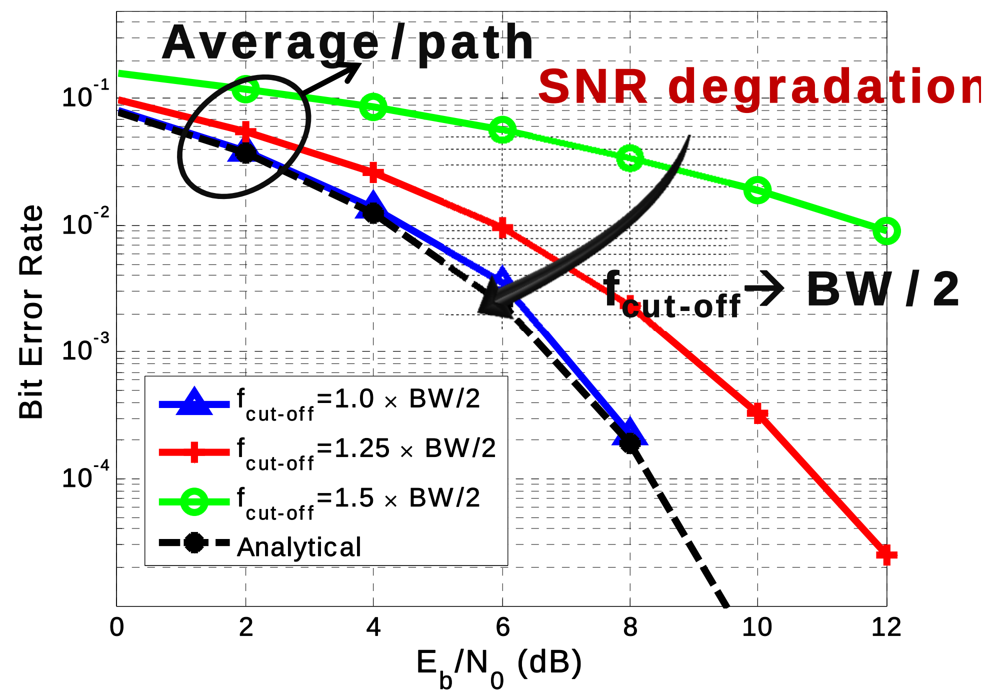


Assumptions

1- LPFs :order 6 (fixed)

2- Vary $f_{cut\text{-}off}$

3-Walsh codes: length 32



Observations:

1- No SNR degradation: LPF $f_{cut\text{-}off}$=BW/2

2- Improve SNR by sacrificing some of the desired signal for less noise and interference (possible for baseband signals)

Conclusion

On-Site Coding Receiver for digital beamforming

→ Use Spreading codes to aggregate all signal paths into a single ADC

→ Hardware Reduction:

- → single ADC
- → Less I/O pins
- → Considerable size, cost, and power reduction

System Considerations

→ Optimal clustering: cost and power reduction

→ Use of Orthogonal codes reduces inter-channel interference

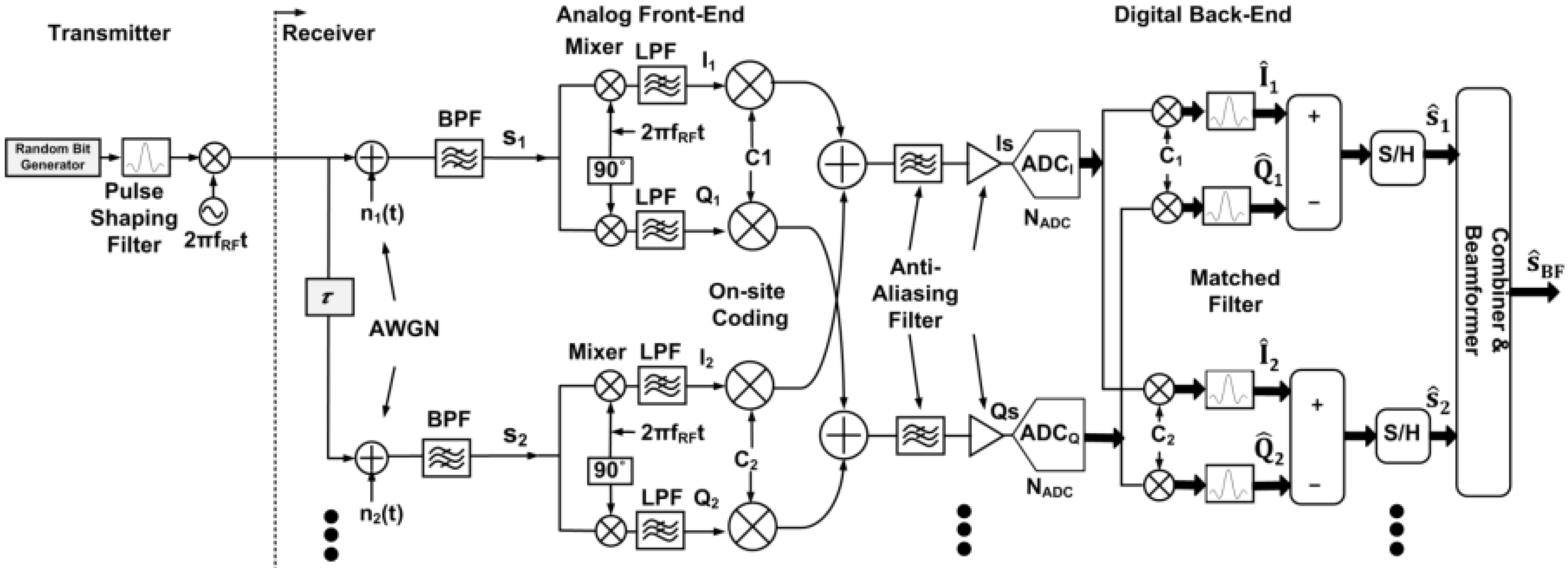
- → Walsh codes with good cross-correlation

→ Cluster size versus ADC speed: cluster size < 1/2 code length

→ Effect of ADC quantization noise: negligible for Nadc>3

→ Design of the analog low pass filter to cancel out undesired signals.

Future Work
Hardware Implementation



- 2-element array antenna and off-the-shelf receiver COTS to demonstrate feasibility of proposed system
- Quadrature-type de-modulation used with direct conversion radio architecture
- On-board PLL used to tune across frequency of interest
- Digital processing using a single FPGA